

arranged in a first direction, (ii) a variable resistance layer formed on the lower electrode line, and (iii) a shared electrode formed in an upper part of the variable resistance layer,

the non-ohmic element including (i) the shared electrode, (ii) one of a semiconductor layer and an insulator layer formed on the shared electrode, and (iii) an upper electrode formed on the one of the semiconductor layer and the insulator layer, and

the method comprising:

forming, on a substrate, a plurality of lower electrode lines in parallel in the first direction;

forming an interlayer insulating layer on the substrate including the lower electrode lines;

forming a plurality of memory cell holes in the interlayer insulating layer formed on the lower electrode lines;

filling an oxide of a transition metal included in the variable resistance layer into the memory cell holes;

forming the shared electrode having a front surface comprising a nitride of the transition metal, by replacing oxygen atoms in a front surface part of the variable resistance layer with nitrogen atoms by nitriding a front surface of the variable resistance layer; and

forming, on the shared electrode and the interlayer insulating layer, the semiconductor or insulator layer and the upper electrode to be shared by, among the non-volatile semiconductor memory elements arranged in the array, non-volatile semiconductor memory elements arranged in a second direction different from the first direction, each of widths of the formed semiconductor or insulator layer and the formed upper electrode being greater than a width of the shared electrode, and each of the semiconductor or insulator layer and the upper electrode being plurally formed in parallel corresponding to the non-volatile semiconductor memory elements arranged in the second direction,

wherein, in the forming of the shared electrode, a front surface of the oxide of the transition metal is nitrided so as to form the shared electrode having a front surface comprising the nitride of the transition metal, and

the front surface of the shared electrode comprises the nitride of the transition metal including the transition metal and nitrogen, so that a Schottky barrier is formed in an interfacial surface between the shared electrode and the semiconductor or insulator layer.

14. The method of manufacturing the non-volatile semiconductor memory device according to claim **13**,

wherein the oxide of the transition metal is one of a tantalum oxide and a hafnium oxide, and

a front surface of the one of the tantalum oxide and the hafnium oxide is nitrided so as to form the shared electrode having a front surface comprising a corresponding one of a tantalum nitride and a hafnium nitride.

15. The method of manufacturing the non-volatile semiconductor memory device according to claim **13**,

wherein the variable resistance layer includes:

a first transition metal oxide layer formed on the first electrode; and

a second transition metal oxide layer that is formed on the first transition metal oxide layer and has a lower oxygen content atomic percentage than the first transition metal oxide layer.

16. A method of manufacturing a cross point non-volatile semiconductor memory device including a plurality of non-

volatile semiconductor memory elements arranged in an array, each of the non-volatile semiconductor memory elements having a variable resistance element and a non-ohmic element connected in series with the variable resistance element,

the variable resistance element including (i) a lower electrode line formed to be shared by, among the non-volatile semiconductor memory elements arranged in the array, non-volatile semiconductor memory elements arranged in a first direction, (ii) a variable resistance layer formed on the lower electrode line, and (iii) a shared electrode formed in an upper part of the variable resistance layer,

the non-ohmic element including (i) the shared electrode, (ii) one of a semiconductor layer and an insulator layer formed on the shared electrode, and (iii) an upper electrode formed on the one of the semiconductor layer and the insulator layer, and

the method comprising:

(a) forming, on a substrate, a plurality of lower electrode lines in parallel in the first direction;

(b) forming a first interlayer insulating layer on the substrate including the lower electrode lines;

(c) forming a plurality of first memory cell holes in the first interlayer insulating layer formed on the lower electrode lines;

(d) filling an oxide of a transition metal included in the first variable resistance layer into the first memory cell holes;

(e) forming a plurality of first shared electrodes by nitriding front surfaces of the plurality of first variable resistance layers;

(f) forming, on the first shared electrode and the first interlayer insulating layer, the first semiconductor or insulator layer and the first upper electrode to be shared by, among the non-volatile semiconductor memory elements arranged in the array, non-volatile semiconductor memory elements arranged in a second direction different from the first direction, each of widths of the formed first semiconductor or insulator layer and the formed first upper electrode being greater than a width of the first shared electrode, and each of the first semiconductor or insulator layer and the first upper electrode being plurally formed in parallel corresponding to the non-volatile semiconductor memory elements arranged in the second direction;

(g) forming an insulation protection layer on an area, out of a region of the first interlayer insulating layer, where the first semiconductor or insulator layer and the first upper electrode are not formed;

(h) forming a second interlayer insulating layer on the insulation protection layer;

(i) forming a plurality of second memory cell holes in the second interlayer insulating layer formed on the first upper electrode;

(j) filling an oxide of a transition metal included in the second variable resistance layer into the second memory cell holes;

(k) forming a plurality of second shared electrodes by nitriding front surfaces of the second variable resistance layers; and

(l) forming, on the second shared electrode and the second interlayer insulating layer, the second semiconductor or insulator layer and the second upper electrode to be shared by, among the non-volatile semiconductor